

FIG. 2

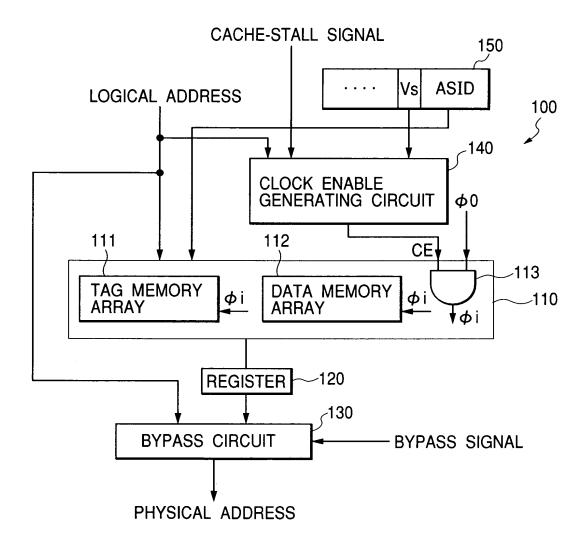


FIG. 3

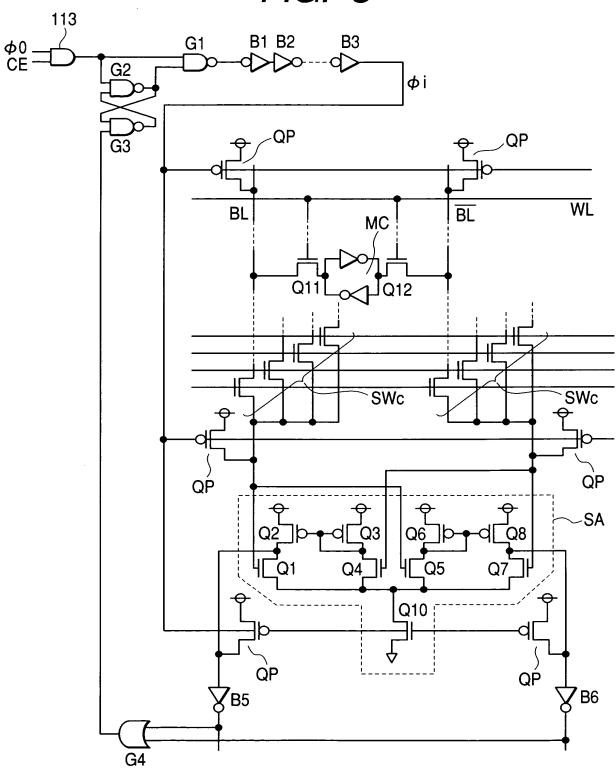


FIG. 4

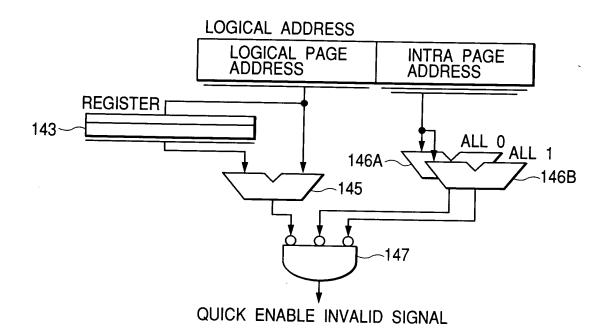


FIG. 5(a)

V-BIT IS 0 IN THE STATUS REGISTER

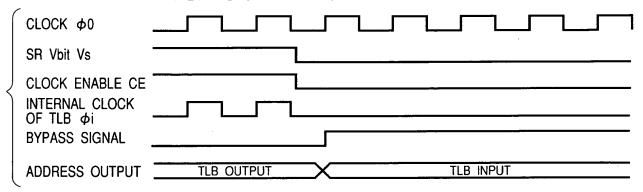


FIG. 5(b)

CACHE-STALL SIGNAL IS HIGH LEVEL

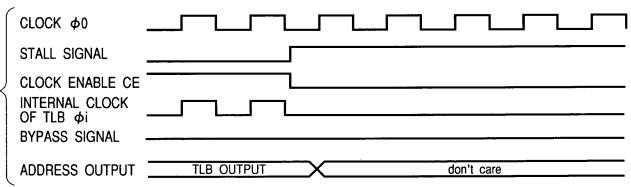
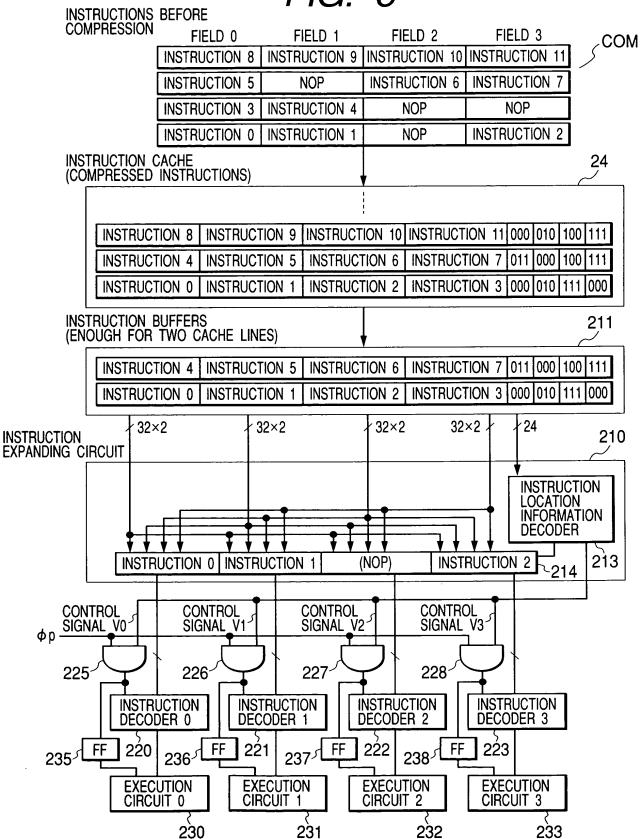


FIG. 5(c)

SAME PAGE ADDRESS IS ACCESSED

CLOCK Ø0		
PAGE ADDRESS	PAGE A	PAGE B
STALL SIGNAL		
CLOCK ENABLE C	E	
INTERNAL CLOCK OF TLB φi		
BYPASS SIGNAL		
ADDRESS OUTPUT	TLB OUTPUT A	TLB OUTPUT B



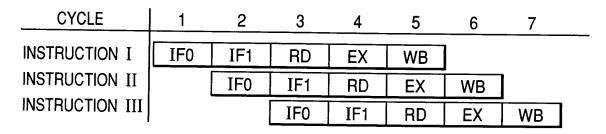


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FIG. 7

INSTRUCTION 4	INSTRUCT	TON 5 I	NSTRUCTIC	N 6	INS	TRUCTION	7 INST	RUCTION ATION DRMATION	
INSTRUCTION 0	INSTRUCT	ION 1 II	1 INSTRUCTION 2 INSTRUC			TRUCTION	3 LOC	INSTRUCTION LOCATION INFORMATION	
LOCATION OF INSTRUCTION 0 (2 BITS)	END INFORMATION OF INSTRUCTION 0 (1 BIT)	LOCATION OF INSTRUCTION 1 (2 BITS)	END INFORMATION OF INSTRUCTION 1 (1 BIT)	LOCATION OF INSTRUCE 2 (2 BIT		END INFORMATION OF INSTRUCTION 2 (1 BIT)	LOCATION OF INSTRUCTION 3 (2 BITS)	END INFORMATION OF INSTRUCTION 3 (1 BIT)	

FIG. 8



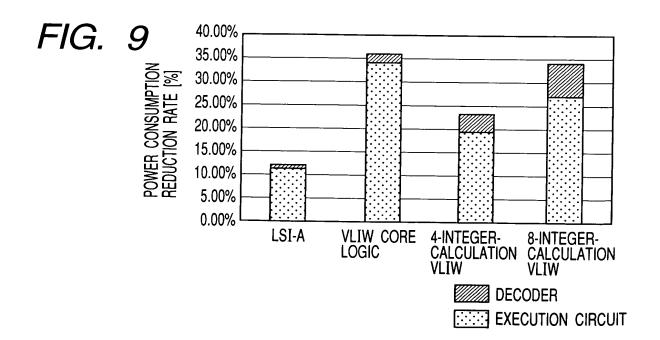


FIG. 10(a)

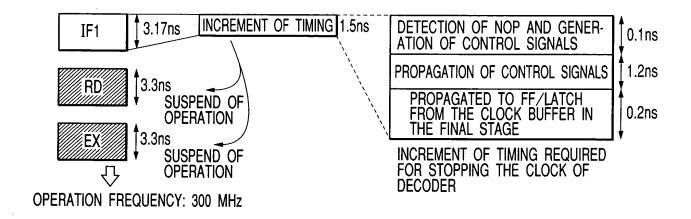


FIG. 10(b)

